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**1  From VHDL to efficient and first-time-right designs: a formal approach**                ■
Peter F. A. Middelhoek, Sreeranga P. Rajan
April 1996  **ACM Transactions on Design Automation of Electronic Systems (TODAES),**
Volume 1 Issue 2

Full text available: 📄 pdf(722.99 KB)   Additional Information: full citation, abstract, references, citings, index terms

> In this article we provide a practical transformational approach to the synthesis of correct synchronous digital hardware designs from high-level specifications. We do this while taking into account the complete life cycle of a design from early prototype to full custom implementation. Besides time-to-market, both flexibility with respect to target architecture and efficiency issues are addressed by the methodology. The utilization of user-selected behavior-preserving transformation steps e ...

> **Keywords:** CDFG, SFG, VHDL, correctness by construction, design methodology, rapid system prototyping, transformational design

**2  Recent developments in high-level synthesis**                ■
Youn-Long Lin
January 1997  **ACM Transactions on Design Automation of Electronic Systems (TODAES),** Volume 2 Issue 1

Full text available: 📄 pdf(232.47 KB)   Additional Information: full citation, abstract, references, citings, index terms

> We survey recent developments in high level synthesis technology for VLSI design. The need for higher-level design automation tools are discussed first. We then describe some basic techniques for various subtasks of high-level synthesis. Techniques that have been proposed in the past few years (since 1994) for various subtasks of high-level synthesis are surveyed. We also survey some new synthesis objectives including testability, power efficiency, and reliability.

> **Keywords:** VLSI design, design automation, design methodology, high level synthesis

**3  Session S3.1: architecture adaptation and synthesis: Cycle-time aware architecture**                ■
**synthesis of custom hardware accelerators**
Mukund Sivaraman, Shail Aditya

Full text available: pdf(75.23 KB)      Additional Information: full citation, abstract, references, index terms

We present the cycle-time aware architecture synthesis methodology used in PICO-NPA that automatically synthesizes minimal cost RT-level designs from high-level specifications to meet a given cycle-time. This allows subsequent physical synthesis to succeed on first pass with predictable performance. The core of the methodology is a static timing analysis engine that is used at multiple levels - program-level, architecture-level and RT-level - in order to identify, schedule and validate useful op ...

**Keywords:** clock frequency, delay analysis, embedded hardware architecture synthesis, high-level synthesis, operator chaining, target clock period, timing analysis, timing during scheduling

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**4** Poster session: An automated and power-aware framework for utilization of IP cores in ▄ hardware generated from C descriptions targeting FPGAs

Alex Jones, Prith Banerjee

Full text available: pdf(187.05 KB)      Additional Information: full citation, abstract

Use of hand optimized Intellectual Property (IP) logic cores is prolific in hardware design. While IP cores remain a standard way to utilize the improvement in FPGA technology and contend with time to market pressure through reuse, popularity of tools generating hardware descriptions from high-level languages is also increasing in popularity. PACT HDL combines these two methods within a power-aware framework. The PACT HDL compiler generates power optimized VHDL/Verilog from a C language descript ...

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**5** An efficient ILP-based scheduling algorithm for control-dominated VHDL descriptions ▄

Michael Münch, Norbert Wehn, Manfred Glesner

Full text available: pdf(375.99 KB)      Additional Information: full citation, abstract, references, index terms

To adopt behavioral synthesis techniques in existing design flows, the synthesis methodology must provide the designer with a mechanism to specify a component's interface timing. This will permit pre- and postsynthesis validation through cosimulation with other subsystems or even through formal verification. In control-flow dominated designs, additional timing constraints will result in a complex specification/constraint system for which the scheduling problem has been shown to be NP-comple ...

**Keywords:** integer linear programming (ILP), scheduling, timing constraints

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**6** Unifying behavioral synthesis and physical design ▄

William E. Dougherty, Donald E. Thomas

Full text available: pdf(397.76 KB)      Additional Information: full citation, abstract, references, citings, index terms

Our methodology unifies behavioral synthesis and physical design, allowing scheduling, allocation, binding, and placement to occur simultaneously. This is accomplished via set of defined transformation from both domains acting as forces in a single behavioral/physical system. Experiments show results with 50% less area and 10% lower critical path delay than the best results from a commercial behavioral synthesis tool. Our behavioral level area,

delay, and individual component locati ...

**Keywords**: behavioral/high level synthesis, physical design

**7** Logic synthesis and mapping: Verifying the correctness of FPGA logic synthesis algorithms

Boris Ratchev, Mike Hutton, Gregg Baeckler, Babette van Antwerpen

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(146.65 KB)    Additional Information: full citation, abstract, references, index terms

Though verification is significantly easier for FPGA-based digital systems than for ASIC or full-custom hardware, there are nonetheless many places for errors to occur.In this paper we discuss the verification problem for FPGAs and describe several methods for verifying end-to-end correctness of synthesis algorithms, a particularly complex portion of the CAD flow. Though the primary contribution of this paper is the analysis of the overall problem, we also give an algorithm for the automatic gen ...

**Keywords**: FPGA, programmable logic, synthesis, test, verification

**8** Poster session: A physical retiming algorithm for field programmable gate arrays

Peter Suaris, Dongsheng Wang, Pei-Ning Guo, Nan-Chi Chou

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB)    Additional Information: full citation, abstract

In this paper, we present a physical retiming algorithm for sequential circuits implemented in field programmable gate arrays (FPGAs). This algorithm can speed up the sequential circuits by reducing delay of all critical paths with negative slacks. By taking advantage of the physical information provided by placed circuits, this algorithm integrates two operations: retiming and register duplication. Retiming moves registers across combinational components. Register duplication moves registers ac ...

**9** Equivalent design representations and transformations for interactive scheduling

Roger P. Ang, Nikil D. Dutt

November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(482.10 KB)    Additional Information: full citation, references, citings, index terms

**10** Poster session: A logic based approach to hardware abstraction

K. Benkrid, S. Belkacemi, D. Crookes

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB)    Additional Information: full citation, abstract

This paper presents a novel approach to hardware abstraction based on the logic programming language Prolog. This is an attempt to satisfy the dual requirement of abstract hardware design and hardware efficiency. Central to this approach is a hardware description environment called HIDE, which provides more abstract hardware descriptions and compositions than are possible in traditional hardware description languages such as VHDL or Verilog. HIDE enables highly scaleable and parameterised compos ...

11

## Poster session: Design strategies and modified descriptions to optimize cipher FPGA implementations: fast and compact results for DES and triple-DES

Gaël Rouvroy, Francois-Xavier Standaert, Jean-Jacques Quisquater, Jean-Didier Legat

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB)    Additional Information: full citation, abstract

We propose a new mathematical DES description that allows optimized implementations. It also provides the best DES and triple-DES FPGA implementations known in term of ratio throughput/area, where area means the number of FPGA slices used. First, we get a less resource consuming unrolled DES implementation that works at data rates of 21.3 Gbps (333 MHz), using VIRTEX II technology. In this design, the plaintext, the key and the mode (encryption/decrytion) can be changed on a cycle-by-cycle basis ...

## 12 Poster session: FPGAs in critical hardware/software systems

Adrian J. Hilton J. Adrian J. Hilton, Gemma Townson, Jon G. Hall

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB)    Additional Information: full citation, abstract

FPGAs are being used in increasingly complex roles in critical systems, interacting with conventional critical software. Established safety standards require rigorous justification of safety and correctness of the conventional software in such systems. Newer standards now make similar requirements for safety-related electronic hardware, such as FPGAs, in these systems. In this paper we examine the current state-of-the-art in programming FPGAs, and their use in conventional (low-criticality) hard ...

## 13 Poster session: Design of a fingerprint system using a hardware/software environment

Lee Vanderlei Bonato, Rolf Fredi Molz, João Carlos Furtado, Marcos Flores Ferrão, Fernando G. Moraes

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB)    Additional Information: full citation, abstract

Processing system of fingerprint are CPU time intensive, being normally implemented in software. This paper present a new algorithm for fingerprint features localization, that can be easily implemented in hardware (system-on-a-chip, FPGA). This algorithm is composed by 3 stages, first stage read a fingerprint image (255x255pixels, ash tones) and apply a Gaussian Filter, after this, apply a absolute difference mask (ADM) for detector the edges in the image filtered and the last stage look for fin ...

## 14 Reconfigurable computing: a survey of systems and software

Katherine Compton, Scott Hauck

June 2002 **ACM Computing Surveys (CSUR)**, Volume 34 Issue 2

Full text available: pdf(710.56 KB)    Additional Information: full citation, abstract, references, citings, index terms, review

Due to its potential to greatly accelerate a wide variety of applications, reconfigurable computing has become a subject of a great deal of research. Its key feature is the ability to perform computations in hardware to increase performance, while retaining much of the flexibility of a software solution. In this survey, we explore the hardware aspects of reconfigurable computing machines, from single chip architectures to multi-chip systems, including internal structures and external coupling. W ...

**Keywords:** Automatic design, FPGA, field-programmable, manual design, reconfigurable architectures, reconfigurable computing, reconfigurable systems

**15** <u>System-level power optimization: techniques and tools</u>

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,
Volume 5 Issue 2

Full text available: <u>pdf(385.22 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

**16** <u>Poster session: Recursive circuit clustering for minimum delay and area</u>

Mehrdad Eslami Dehkordi, Stephen D. Brown

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: <u>pdf(187.05 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>

We present an effective recursive algorithm for circuit clustering for delay and area minimization, which is applicable to FPGAs. At the highest level of clustering, the circuit is clustered using a modified single-level clustering algorithm. A cluster to netlist transformation technique is proposed, which converts each cluster into a new subcircuit. The algorithm then continues recursively by clustering the generated subcircuits into further levels of clusters. To reduce the amount of node dupl ...

**17** <u>Poster session: Making area-performance tradeoffs at the high level using the AccelFPGA compiler for FPGAs</u>

P. Banerjee, V. Saxena, J. Uribe, M. Haldar, A. Nayak, V. Kim, D. Bagchi, S. Pal, N. Tripathi, R. Anderson

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: <u>pdf(187.05 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>

Applications such as digital cell phones, 3G wireless receivers, and voice over IP, require DSP functions that are typically mapped onto general purpose DSP processors. With the introduction of advanced FPGA architectures which provide built-in DSP support such as the Xilinx Virtex-II, and the Altera Stratix, a new hardware alternative is available for DSP designers. DSP design has traditionally been divided into algorithm development and hardware/software implementation. The majority of DSP alg ...

**18** <u>Poster session: Wireless sensor networks: a power-scalable motion estimation IP for hybrid video coding</u>

Federico Quaglio, Maurzio Martina, Fabrizio Vacca, Guido Masera, Andrea Molino, Gianluca Piccinini, Maurizio Zamboni

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: <u>pdf(187.05 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>

Wireless Sensor Networks are an emerging phenomenon in the research community. The design and development of network architectures and nodes implementation are fostering many research activities. Due to their wide application fields and pervasive employment possibilities, the investigation of novel classes of wireless sensor nodes is of great concern. In this paper we presented a novel Power-Scalable Motion Estimation IP suitable for video-surveillance over Wireless Sensor Networks. The proposed ...

**19** <u>Poster session: Reconfigurable randomized K-way graph partitioning</u>

Fatih Kocan

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: <u>pdf(187.05 KB)</u>    Additional Information: <u>full citation</u>, <u>abstract</u>

In this paper, a randomized k-way graph partitioning algorithm is mapped onto reconfigurable hardware. The randomized algorithm relies on repetitive running of the same algorithm with different random number sequences to achieve the (near-)optimal solution. The run-time and hardware requirements of this reconfigurable solution per a random number sequence are $O(|V|-K)$ cycles and $O(|V|\log|V|+|E|)$ gates and flip-flops, respectively. Performance is improved further at the expense of more hardware b ...

**20** <u>Poster session: On hiding latency in reconfigurable systems: the case of merge-sort for an FPGA-based system</u>

Hossam ElGindy, George Ferizis

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: <u>pdf(187.05 KB)</u>    Additional Information: <u>full citation</u>, <u>abstract</u>

Recursive solutions are effective software techniques that are difficult to map into hardware due to their dependency on input size and data values. As a result, most high-level design tools do not allow for recursive calls. In this paper we present a technique for mapping the merge-sort algorithm, as a case study, into a reconfigurable system. Our mapping employs an on-line prediction method to reconfigure the necessary hardware only when the need arises, and to hide the reconfiguration delay. ...

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**5 Low power register allocation algorithm using graph coloring**
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[Abstract]   [PDF Full-Text (336 KB)] **IEEE CNF**

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**6 Efficient hardware controller synthesis for synchronous dataflow graph in system level design**
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System Synthesis, 2000. Proceedings. The 13th International Symposium on , 20-22 Sept. 2000
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[Abstract]   [PDF Full-Text (484 KB)] **IEEE CNF**

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**7 Efficient hardware controller synthesis for synchronous dataflow graph in system level design**
*Hyunuk Jung; Kangnyoung Lee; Soonhoi Ha;*
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 Issue: 4 , Aug. 2002
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[Abstract]   [PDF Full-Text (324 KB)] **IEEE JNL**

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US-PAT-NO: 6021266
DOCUMENT-IDENTIFIER: US 6021266 A

TITLE: Method of designing an integrated circuit using scheduling and allocation with parallelism and handshaking communication, and an integrated circuit designed by such method

DATE-ISSUED: February 1, 2000

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|------|------|-------|----------|---------|
| Kay; Andrew | Oxford | | | GB |

US-CL-CURRENT: 716/2; 716/1, 717/143, 717/154

ABSTRACT:

An integrated circuit is designed by defining its functions in a programming language which supports parallelism and synchronized communication. The resulting source code is supplied to a compiler which includes an optimizer module for retiming synchronized communication without changing the order of external communications of the integrated circuit. The compiler produces output code which represents the circuitry of the integrated circuit and which may be supplied to synthesis tools and subsequent steps in the manufacture of the integrated circuit.

13 Claims, 19 Drawing figures
Exemplary Claim Number: 11
Number of Drawing Sheets: 9